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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/786,296	02/26/2004	Nobuhiro Nishikawa	103213-00072	3437

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EXAMINER	
NADAV, ORI	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 03/15/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/786,296	NISHIKAWA ET AL.	
	Examiner	Art Unit	
	ori nadav	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 March 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 and 3-7* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 and 3-7* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d)

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date _____
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other _____

DETAILED ACTION

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 1 and 3-7 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. The specification describes a load being connected to a connection portion between the first conductive region of the first MOS transistor and ground. There is no support in the specification for a load being connected to a connection portion between the first conductive region of the first MOS transistor and the third conductive region of the second MOS transistor, as recited in claims 1 and 5.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1 and 3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Heuner et al. (4,066,918) in view of McDaniel (5,243,236).

Regarding claims 1 and 3, Heuner et al. teach in figure 2 and related text a semiconductor integrated circuit device comprising:

A first MOS transistor N1 having a first backgate region 305, a first conductive region 233, and a second conductive region 235, and having the first backgate region and the first conductive region thereof connected together;

a second MOS transistor P1 having a second backgate region 330, a third conductive region 221, and a fourth conductive region 223, having the second backgate region and the third conductive region thereof connected to the first backgate region and the first conductive region of the first MOS transistor (via diode D5, see figure 1), and receiving at the fourth conductive region thereof a first direct-current voltage;

a voltage setting circuit R1 setting a second direct-current voltage fed to a gate of the second MOS transistor; and

an anti-reverse-current element D12, D22 receiving the first direct-current voltage or a third direct-current voltage produced from the first direct-current voltage, and connected to the voltage setting circuit in such a way as to prevent a reverse current from flowing through the voltage setting circuit,

wherein the voltage setting circuit produces, according to the first direct- current voltage or the third direct-current voltage, the second direct-current voltage within a withstand voltage range of the second MOS transistor, and wherein, between the first backgate

region and the second conducting region of the first MOS transistor, a first parasitic diode is formed and. between the second backgate region and the fourth conducting region of the second MOS transistor, a second parasitic diode is formed.

Note that the broad recitation of the claim does not require the second backgate region and the third conductive region thereof to be directly connected to the first backgate region, and does not require the first direct- current voltage to be a different voltage than the second direct-current voltage.

Heuner et al. do not teach first and second MOS transistors having the same polarity, and a load being connected to a connection portion between the first conductive region of the first MOS transistor and the third conductive region of the second MOS transistor. McDaniel teaches in figure 5 first and second MOS transistors having the same polarity. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use first and second MOS transistors having the same polarity and a load being connected to a connection portion between the first conductive region of the first MOS transistor and the third conductive region of the second MOS transistor in Heuner et al.'s device in order to use the device in an application which requires two transistors of the same polarity, and in order to adjust the voltage characteristics of the device by forming a load between the voltage source and the ground.

Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Heuner et al. and McDaniel, as applied to claim 1 above, and further in view of Stewart (3,967,295).

Regarding claim 4, Heuner et al. and McDaniel teach substantially the entire claimed structure, as applied to claim 1 above, except a voltage setting circuit being composed of voltage-division resistors.

Stewart teaches in figure 3 a voltage setting circuit being composed of voltage-division resistors. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use a voltage setting circuit being composed of voltage-division resistors in Heuner et al. and McDaniel's device in order to better control the voltage distribution of the device.

Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Heuner et al. and McDaniel, as applied to claim 1 above, and further in view of in view of Stewart (3,967,295).

Regarding claim 5, Heuner et al. and McDaniel teach substantially the entire claimed structure, as applied to claim 1 above, except a voltage setting circuit being having one end thereof grounded.

Stewart teaches in figure 3 a voltage setting circuit having one end thereof grounded. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use a voltage setting circuit having one end thereof grounded in Heuner et al. and McDaniel's device in order to better control the voltage distribution of the device.

Note that the broad recitation of the claim does not require the second backgate region and the third conductive region thereof to be directly connected to the first backgate

region, and does not require the first direct- current voltage to be a different voltage than the second direct-current voltage.

Response to Arguments

Applicant's arguments with respect to claims 1 and 3-7 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Papers related to this application may be submitted to Technology center (TC) 2800 by facsimile transmission. Papers should be faxed to TC 2800 via the TC 2800 Fax center located in Crystal Plaza 4, room 4-C23. The faxing of such papers must conform with the notice published in the Official Gazette, 1096 OG 30 (November 15, 1989). The Group 2811 Fax Center number is (703) 308-7722 and 308-7724. The Group 2811 Fax Center is to be used only for papers related to Group 2811 applications.

Any inquiry concerning this communication or any earlier communication from the Examiner should be directed to *Examiner Nadav* whose telephone number is **(571) 272-1660**. The Examiner is in the Office generally between the hours of 7 AM to 4 PM (Eastern Standard Time) Monday through Friday.

Any inquiry of a general nature or relating to the status of this application should be directed to the **Technology Center Receptionists** whose telephone number is **308-0956**

O.N.
3/9/05

ORI NADAV
PRIMARY EXAMINER
TECHNOLOGY CENTER 2800